ACCELERATED LIFE TEST OF MRAM CELLS

Abstract of the Disclosure

A circuit provides a stress voltage to magnetic tunnel junctions (MTJs), which comprise the storage elements of a magnetoresitive random access memory (MRAM), during an accelerated life test of the MRAM. The stress voltage is selected to provide a predetermined acceleration of aging compared to normal operation. A source follower circuit is used to apply a stress voltage to a subset of the memory cells at given point in time during the life test. The stress voltage is maintained at the desired voltage by a circuit that mocks the loading characteristics of the portion of the memory array being stressed. The result is a closely defined voltage applied to the MTJs so that the magnitude of the acceleration is well defined for all of the memory cells.